REMARKS

The above Amendments and these Remarks are in reply to the Office action mailed February 9, 2006.

Currently, claims 1-55 are pending. Applicants have amended claims 1, 5, 9, 12, 15, 16, 18-24, 28-31, 33, 35, 36, 40, and 52-55, cancelled claims 13, 26, 43, and 48-51, and added claims 56-59. Applicants respectfully request reconsideration of claims 1-12, 14-25, 27-42, 44-47, and 52-55 and consideration of newly added claims 56-59.

I. Objection to Drawings

Figures 1-4 were objected to for not including a legend such as "Prior Art." Figures 1-4 have been amended to include a legend designating each figure as prior art. Replacement drawing sheets are submitted herewith. It is respectfully submitted that the amended drawings overcome the objection and are in compliance with MPEP § 608.02(g).

II. Objection to Specification

Claim 26 was objected to for reciting "a second group." Claim 26 has been cancelled.

III. Allowable Subject Matter

Claims 4-7, 9-10, 17, 19-21, 38, and 40-42 were objected to as being dependent upon a rejected base claim, but indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 has been rewritten in independent form and includes all the limitations of independent base claim 1 and intervening dependent claim 2. Applicant respectfully submits that claim 5 is in condition for allowance. Claims 6-7 each ultimately depend from claim 5 and should be allowable for at least the same reasons as claim 5.

Claim 9 has been rewritten in independent form and includes all the limitations of independent base claim 1 and intervening dependent claim 2. Applicant respectfully submits that claim 9 is in condition for allowance. Claim 10 depends from claim 9 and should be allowable for at least the same reasons as claim 9.

Claim 40 has been rewritten in independent form and includes all the limitations of independent base claim 33 and intervening dependent claim 34. Applicant respectfully submits that claim 40 is in

condition for allowance. Claims 41-42 each ultimately depend from claim 40 and should be allowable for at least the same reasons as claim 40.

Claims 4, 17, 19-21, and 38 each ultimately depend from an independent claim which is asserted to be patentable over the cited art under § 102(e) as set forth below.

IV. Rejection of Claims 1-3, 8, 11-16, 18, 22-37, 39 and 43-55 under 35 U.S.C 102(e)

Claims 1-3, 8, 11-16, 18, 22-37, 39 and 43-55 were rejected under 35 U.S.C 102(e) as being anticipated by U.S. Patent No. 6,859,397 *(Lutze)*. Claims 13, 26, 43, and 48-51 have been cancelled. Because the prior art fails to disclose each of the limitations of claims 1-3, 8, 11, 12, 14-16, 18, 22-25, 27-37, 39, 44-47, and 52-55, Applicant respectfully submits that these claims are patentable under § 102(e).

Claims 1-3, 8, 11, 12, 14-16, 18, 22-25, and 27-32

Independent claim 1 has been amended and now recites:

> boosting a voltage potential of a channel of a first plurality of non-volatile storage elements including a storage element to be inhibited from programming, each storage element of said first plurality is in communication with a first bit line receiving an inhibit voltage during said inhibiting;
>
> inhibiting programming of a second plurality of non-volatile storage elements during at least a portion of said boosting, said second plurality including a storage element to be programmed, each storage element of said second plurality is in communication with a second bit line receiving an inhibit voltage during said inhibiting;
>
> trapping at least a portion of said voltage potential in a portion of said channel associated with a first subset of said first plurality of non-volatile storage elements; and
>
> enabling programming of said second plurality of non-volatile storage elements subsequent to said step of trapping by applying a program enable voltage on said second bit line.

Applicant respectfully submits that the amendments to claim 1 overcome the rejection of claim 1 under § 102(e). The rejection of claim 1 relied upon the "unselected word lines" and the "selected word line" of the cited art as the "first group" (amended herewith to recite "first plurality") and the "second group" (amended herewith to recite "second plurality"), respectively. Applicant notes that the storage elements connected to a word line in the cited art are not each "in communication with a first bit line," as required of the "first plurality" of elements and the "second plurality" of elements in amended claim 1.

Rather, each storage element of a particular word line is in communication with a different bit line. This architecture is well described in both the cited art (*see e.g., Lutze, Figure 4 and col. 2, ll. 19-47*) and *Applicant's Specification* (*see e.g., Figure 4 and ¶ 0006*). Therefore, the storage elements of a particular word line cannot disclose a "first plurality" of storage elements that are each "in communication with a first bit line" or a "second plurality" of storage elements that are each "in communication with a second bit line," as recited in claim 1.

Applicant further notes that claim 1 recites "inhibiting programming of a second plurality of non-volatile storage elements during at least a portion of said boosting, said second plurality including a storage element to be programmed." The cited art does not disclose inhibiting programming of *a storage element to be programmed* during boosting as required in claim 1. The cited art discloses that the "bit line for the cell being programmed is at ground and the bit line of the string with the cell being inhibited is at Vdd." *Col. 4, ll. 4-7; see also, col. 11, ll. 57-59 and Figures 14-18.* The cited art does not disclose that the bit line of the cell to be programmed is at Vdd to inhibit programming.

Because the prior art fails to disclose each of the limitations of claim 1, Applicant asserts that claim 1 is patentable under § 102(e). Claims 3, 8, 11, 12, 14-16, 18, 22-25, and 27-32 each ultimately depend from claim 1 and therefore, should be patentable for at least the same reasons.

Claims 33-37, 39, and 44-47

Independent claim 33 has been amended and now recites, among other limitations:

> a plurality of word lines coupled to said first group and said second group to apply one or more boosting voltages to raise a voltage potential of a channel of said first group, said plurality of word lines includes a first word line coupled to said storage element to be inhibited and to said storage element to be programmed, said first word line applies a program voltage to said storage element to be programmed during a program operation, said plurality of word lines includes *a first bounding word line on a source side of said first word line and a second bounding word line on a drain side of said first word line, said first and second bounding word lines have said one or more boosting voltages lowered thereon, prior to applying said program voltage on said first word line,* in order to trap said voltage potential in a portion of said channel associated with said first subset of said first group. (*Emphasis added*)

Claim 33 now requires "a first bounding word line on a source side" of the word line applying the program voltage and "a second bounding word line on a drain side" of the word line applying the

program voltage, wherein both bounding word lines "have said one or more boosting voltages lowered thereon." The cited art does not disclose such a configuration of bounding word lines. The rejection of claim 33 cites the "WL [word line] source side neighbor" in Figures 14-18 of the cited art which is raised to Vssb and then lowered to Vss. On the drain side, however, there is no such lowering. The "unselected WL drain side" voltage is raised to Vpass as the program voltage Vpgm is applied. This voltage remains at Vpass and is not shown to be lowered "prior to applying said program voltage on said first word line," as recited in claim 33. Thus, the cited art fails to disclose "a second bounding word line on a drain side of said first word line" that has "said one ore more boosting voltages lowered thereon, prior to applying said program voltage on said first word line."

Because the prior art fails to disclose each limitation of claim 33, Applicant asserts that claim 33 is patentable under § 102(e). Claims 34-37, 39, and 44-47 each ultimately depend from claim 33 and therefore, should be patentable for at least the same reasons.

Claim 52

Claim 52 has been amended and now recites, among other limitations:

> *boosting a voltage potential of a channel of a first group of non-volatile storage elements and a channel of a second group of non-volatile storage elements* by applying a first boosting voltage to a first plurality of word lines and a second boosting voltage to a second plurality of word lines, *said first group includes a storage element to be programmed* and said second group includes a storage element to be inhibited from programming,
>
> ...
>
> programming said storage element to be programmed subsequent to said step of lowering said second boosting voltage, *said programming includes draining at least a portion of said boosted voltage potential from said channel of said first group.* (*Emphasis added*)

Claim 52, as amended, includes a boosting limitation that comprises boosting a voltage potential of "a channel of a first group of non-volatile storage elements" that includes "a storage element to be programmed." Claim 52 further recites the limitation that "programming includes draining at least a portion of said boosted voltage potential from said channel of said first group." The cited art does not disclose "boosting a voltage potential of a channel of a first group" and then "draining at least a portion of said boosted voltage potential" during programming. Thus, the addition of these limitations to claim 52 overcomes the rejections based on the cited art.

Because the prior art fails to disclose each limitation of claim 52, Applicant asserts that claim 52 is patentable under § 102(e).

Claim 53

Claim 53 has been amended and now recites, among other limitations:

> inhibiting programming of a first plurality of non-volatile storage elements and a second plurality of non-volatile storage elements by applying a program inhibit voltage to a bit line in communication with each storage element of said first plurality and applying a program inhibit voltage to a second bit line in communication with each storage element of said second plurality, said first plurality including a non-volatile storage element to be inhibited, said second plurality including a non-volatile storage element to be programmed;
>
> applying a first boosting voltage to a first subset of non-volatile storage elements of said first plurality and a second boosting voltage to a second subset of non-volatile storage elements of said first plurality to boost a voltage potential of a channel of said first plurality of non-volatile storage elements;
>
> applying said first boosting voltage to a third subset of non-volatile storage elements of said second plurality and said second boosting voltage to a fourth subset of non-volatile storage elements of said second plurality to boost a voltage potential of a channel of said second plurality of non-volatile storage elements, said applying said first boosting voltage and said second boosting voltage is performed while inhibiting programming of said second plurality including said non-volatile storage element to be programmed;
>
> ...
>
> applying a program enable voltage to said second bit line subsequent to said step of lowering said second boosting voltage.

Claim 53 now recites limitations similar to those of claim 9 and claim 40 which were both indicated to include allowable subject matter. For example, claim 53 recites "applying said first boosting voltage to a third subset of non-volatile storage elements of said second plurality and said second boosting voltage to a fourth subset of non-volatile storage elements of said second plurality," similarly to claim 9. Claim 53 further recites "applying a program enable voltage to said second bit line subsequent to said step of lowering said second boosting voltage," similarly to claim 40. Claim 53 also recites inhibiting programming of "a second plurality of non-volatile storage elements" that includes "a non-volatile storage element to be programmed," similarly to claim 1. Accordingly, for at least the same reasons set forth above with respect to claims 1, 9, and 40 and as noted by the Examiner in the indication of allowable subject matter, Applicant asserts that claim 53 is patentable under § 102(e) over the cited

art. Claims 54 and 55 each ultimately depend from claim 53 and therefore, should be patentable for at least the same reasons.

V. Newly Added Claims

Claims 56-59 have been added. Claims 56-57 each depend from claim 9 and claims 58-59 each depend from claim 40. Applicant respectfully submits that each of these claims is patentable over the cited art for at least the same reasons as the respective independent claim from which it depends.

VI. Conclusion

Based on the above amendments and these remarks, reconsideration of claims 1-12, 14-25, 27-42, 44-47, and 52-55 and consideration of newly added claims 56-59 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, August 7, 2006.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

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